


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☐ The ACM Digital Library ☒ The Guide

extracting logic element

SEARCH

THE GUIDE TO COMPUTING LITERATURE

 Feedback [Report a problem](#) [Satisfaction survey](#)

 Terms used extracting logic element

Found 52,754 of 887,066

Sort results by

relevance

☒ [Save results to a Binder](#)

 Try an [Advanced Search](#)

Display results

expanded form

☐ [Search Tips](#)

 Try this search in [The Digital Library](#)
☐ Open results in a new window

Results 1 - 20 of 200

 Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

 Relevance scale ☐ ☐ ☐ ☐ ☐

1 [High capacity and automatic functional extraction tool for industrial VLSI circuit designs](#)

Sasha Novakovsky, Shy Shyman, Ziyad Hanna

 November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

 Full text available: [pdf\(95.14 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we present an advanced functional extraction tool for automatic generation of high-level RTL from switch-level circuit netlist representation. The tool is called FEV-Extract and is part of a comprehensive Formal Equivalence Verification (FEV) system developed at Intel to verify modern microprocessor designs. FEV-Extract employs a powerful hierarchical analysis procedure, and advanced and generic algorithms for automatic recognition of logical primitives, to cope with variety of cir ...

Keywords: Binary Decision Diagrams (BDDs), Design For Testability (DFT), Formal Equivalence Verification (FEV), Hardware Description Languages (HDL), Switch Level Analysis, functional abstraction, logic simulation, satisfiability procedures, synthesis

2 [Precise timing verification of logic circuits under combined delay model](#)

Shinji Kimura, Shigemi Kashima, Hiromasa Haneda

 November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

 Full text available: [pdf\(447.97 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

3 [Defect Detection from Visual Abnormalities in Manufacturing Process Using IDDQ](#)

Masaru Sanada

 June 2001 **Journal of Electronic Testing: Theory and Applications**, Volume 17 Issue 3-4

Publisher: Kluwer Academic Publishers

 Full text available: [Publisher Site](#) Additional Information: [full citation](#), [abstract](#)

Abnormal I_{DDQ} (Quiescent V_{DD} supply current) indicates the existence of physical damage in a circuit. Using this phenomenon, a CAD-based fault diagnosis technology has been developed to enhance the manufacturing yield of logic LSI. This method to detect the fatal defect fragments in several abnormalities identified with wafer inspection apparatus includes a way to separate various leakage faults, and to define the diagnosis area encircling the abnormal port ...